WHAT IS CLAIMED IS:

1. A method of forming an electrical fuse, the method comprising the steps of:

providing a semiconductor-on-insulator wafer having a first layer, an insulator layer, and an active layer;

etching the active layer of a semiconductor-on-insulater wafer to form the electrical fuse;

doping the electrical fuse; and

siliciding the surface of the electrical fuse.

2. The method of claim 1, wherein the electrical fuse comprises a thin conductive strip between two wider conductive areas.

3. The method of claim 1, wherein the step of doping is performed such that the electrical fuse is fully depleted.

4. The method of claim 1, further comprising the step of forming a spacer around the circumference of the electrical fuse.

5. The method of claim 1, wherein the step of siliciding the surface of the electrical fuse is performed by depositing a metal and performing an anneal.

6. The method of claim 1, wherein the step of etching the active layer to form the electrical fuse includes etching the active layer to form a source/drain region of a transistor.

7. The method of claim 6, wherein the transistor is a FinFET.

8. A method of forming a semiconductor device, the method comprising the steps of:

providing a substrate, the substrate having a first layer, an insulator layer formed on the first layer, and an active layer formed on the insulator layer;

simultaneously forming a source/drain region of a transistor and an electrical fuse in the active layer;

forming a gate electrode of the transistor on the source/drain region;

forming lightly-doped drain regions in the source/drain region;

forming spacers along the side of the gate electrode; and

implanting exposed portions of the source/drain regions and the electrical fuse such that the exposed portions of the source/drain regions and the electrical fuse are substantially fully depleted.

9. The method of claim 8, further comprising the step of siliciding the surface of at least one of the gate electrode, source/drain region, and the electrical fuse.

10. The method of claim 8, wherein the electrical fuse comprises a thin conductive strip between two wider conductive areas.

11. The method of claim 8, further comprising siliciding a surface of the electrical fuse by depositing a metal and performing an anneal.

12. The method of claim 8, wherein the transistor is a FinFet.

13. An electrical fuse comprising:

a first section;

a second section; and

a third section electrically coupled to the first section and the second section;

wherein the first section, the second section, and the third section are formed from an active layer of a semiconductor-on-insulator, and at least a portion of the surface of the first section, the second section, and the third section are silicided.

14. The electrical fuse of claim 13, wherein the first section, the second section, and the third section are fully depleted.

15. The electrical fuse of claim 13, wherein the third section is narrower than at least one of the first section and the second section.

16. The electrical fuse of claim 13, further comprising a spacer formed along the perimeter of the electrical fuse.

17. A semiconductor device comprising:

a transistor having a source/drain region formed on a substrate and a gate electrode formed on the source/drain region; and

an electrical fuse having a first section and a second section interconnected by a third section, the third section being narrower than at least one of the first section and the second section;

wherein the electrical fuse and the source/drain region are formed in an active layer of a silicon-on-insulator substrate.

18. The electrical fuse of claim 17, wherein the first section, the second section, and the third section are fully depleted.

19. The electrical fuse of claim 17, wherein a surface of the electrical fuse is silicided.

20. The electrical fuse of claim 17, further comprising a spacer formed along the perimeter of the electrical fuse.

21. The electrical fuse of claim 17, wherein the transistor is a FinFET.